



Development of thin pixel sensors and a novel interconnection technology for the SLHC

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on behalf of

MPI Munich SLHC Upgrade Group

- ✓ *Upgrade of the ATLAS pixel system at Super-LHC*
- ✓ *Properties of thin sensors*
- ✓ *The 3D integration approach at Fraunhofer-IZM*
 - Solid Liquid Inter Diffusion (SLID)*
 - Inter Chip Vias (ICV)*
- ✓ *New production of thin pixels sensors at MPI-HLL*
- ✓ *First checks of the SLID process on test diodes*



The Challenge

Expected conditions at LHC and Super-LHC

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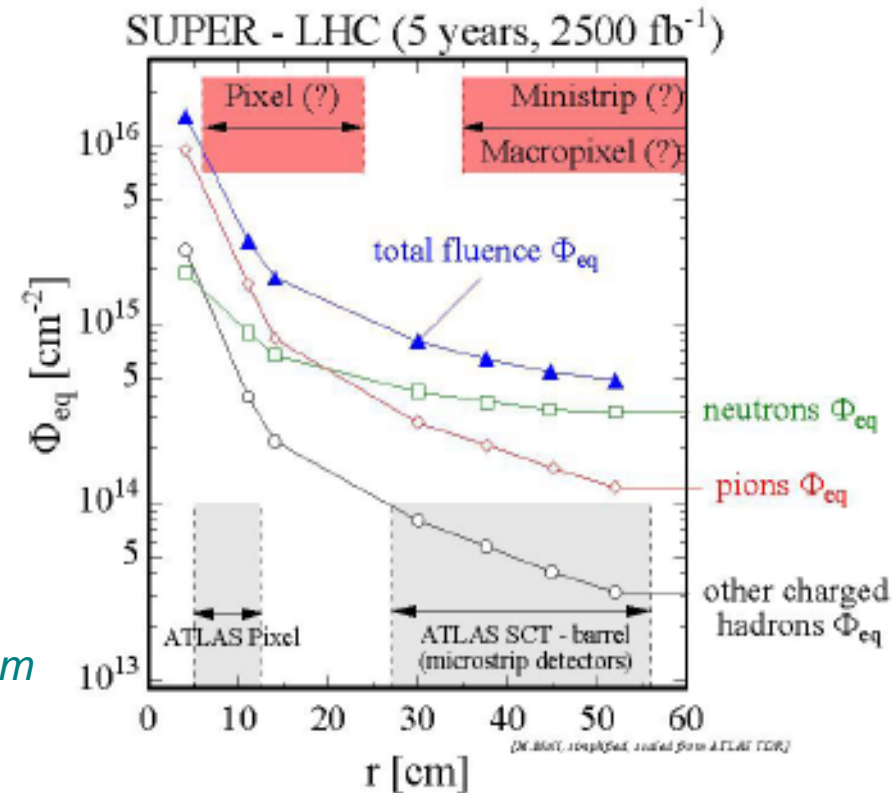
LHC:

- Start 2008
- $L = 10^{34} \text{cm}^{-2} \text{s}^{-1}$
- Integrated Luminosity: 500fb^{-1} (10y)
- $\Phi = 3 \times 10^{15} \text{cm}^{-2}$ 1 MeV eq. n at $r=4\text{cm}$
- Multiplicity: 0.5-1 k tracks/event

Super-LHC:

- Start 2013-2016
- $L = 10^{35} \text{cm}^{-2} \text{s}^{-1}$
- Integrated Luminosity: 2500fb^{-1} (5y)
- $\Phi = 1.6 \times 10^{16} \text{cm}^{-2}$ 1 MeV eq. n at $r=4\text{cm}$
- Multiplicity: 5-10 k tracks/event

New detector concepts needed!





The ATLAS Pixel Detector

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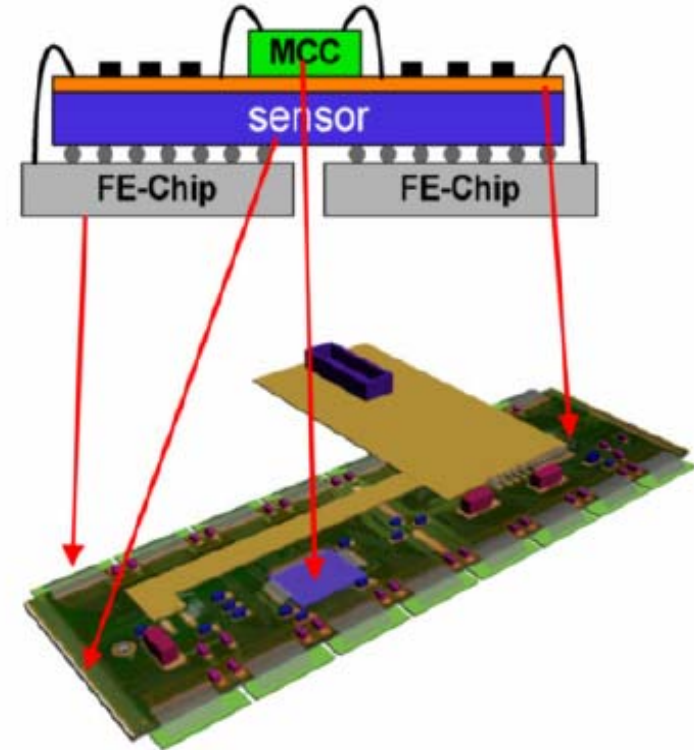
Present Layout:

- 250 μm *n-in-n* pixel sensor
- 50 x 400 μm^2 pixels
- 0.25 μm rad hard ASIC
- rad hard till 10^{15} n/cm²

- Live fraction ~71%
- Cantilever for readout
- Sensor width 2x chip size: 16 mm
- Large material overhead

Expected at SLHC:

- It should work in undepleted mode ($V_{\text{dep}} \sim 4200\text{V}$)
- Charge Collection Efficiency: ~15% @ 10^{16} n/cm²
- High occupancy



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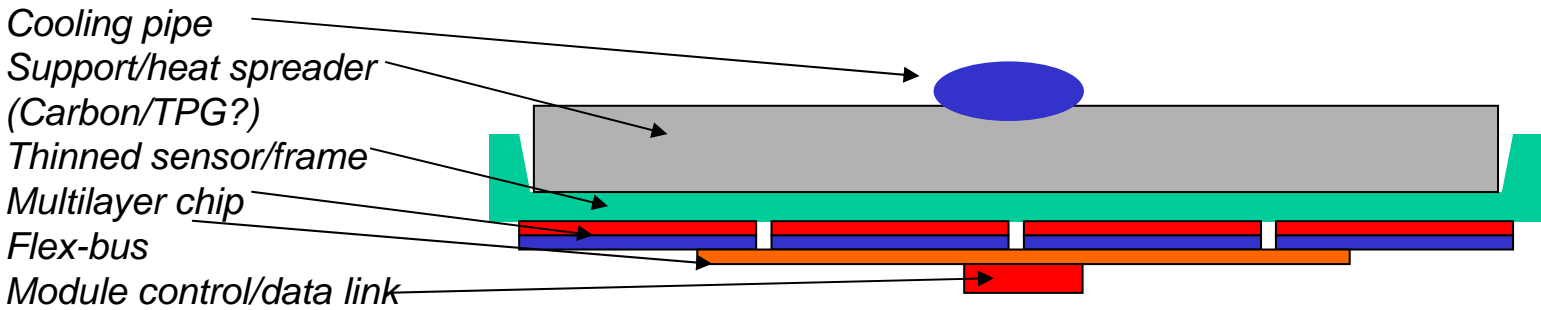
Main cost driver: Bump bonding !



Conceptual Module Design

Work on conceptual module design using 3D interconnection technologies:

- ✓ *Thinned pixel sensors* → *Improved radiation hardness*
- ✓ *SLID connection between thin pixel sensors and front-end* → *smaller pitches possible*
- ✓ *Stacked layers of electronics, for example digital read-out on top of the analogue layer* → *different technologies can be used and singularly optimized*
- ✓ *Route signals through vias across the Si layers* → *avoid need of cantilever → four side buttable*

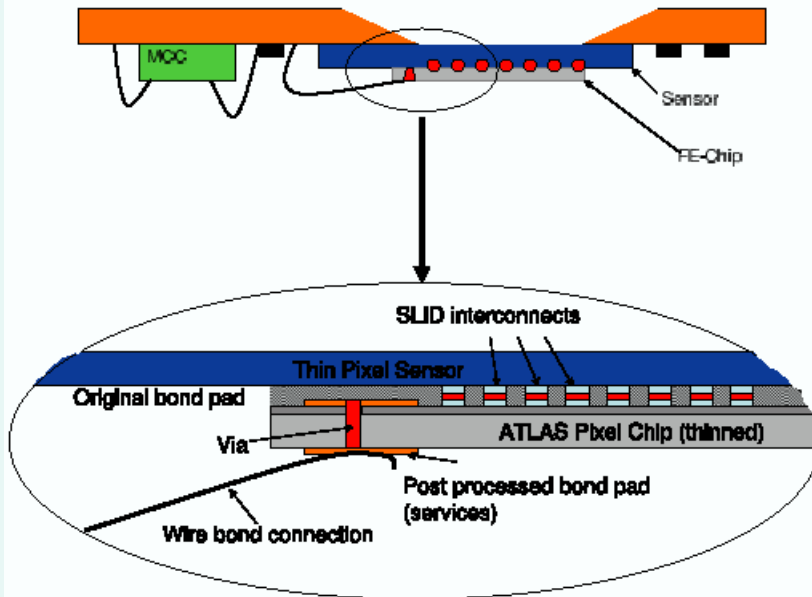




Envisaged Demonstrator Module

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First module demonstrator (2007-2009)



It should allow us to test:

- ✓ *Thin sensors*
- ✓ *SLID connection between pixel sensors and ASIC, placed face to face*
- ✓ *Thinning of the readout chip wafer*
- ✓ *drilling of vias to route signal and services out from the ASIC wafer backside*

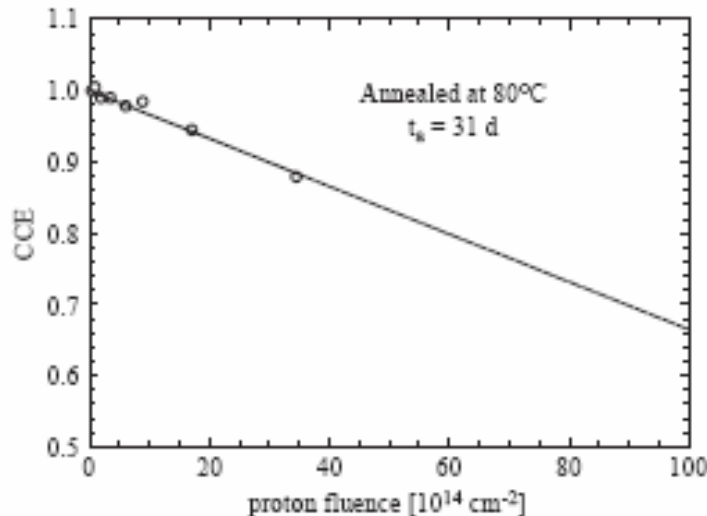
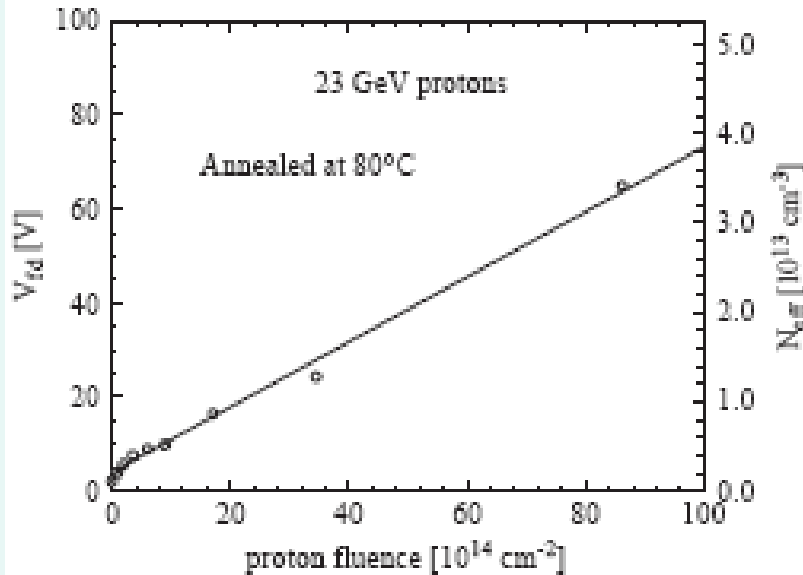
✓ *Collaboration with Bonn, Dortmund and Oslo Universities within the ATLAS experiment to fully characterize the demonstrator module.*



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Why thin pixels for SLHC?



*For 50 μ m thick Fz diodes
processed at MPI*

✓ *after short term annealing*

$V_{dep} < 100V$ at 10^{16} p/cm 2

✓ *Leakage currents:*

$\alpha(80^\circ C, 8min) = 4.3 \times 10^{-17}$ A/cm.

✓ *CCE ~ 66% @ 10^{16} p/cm 2 (extrapolated)*

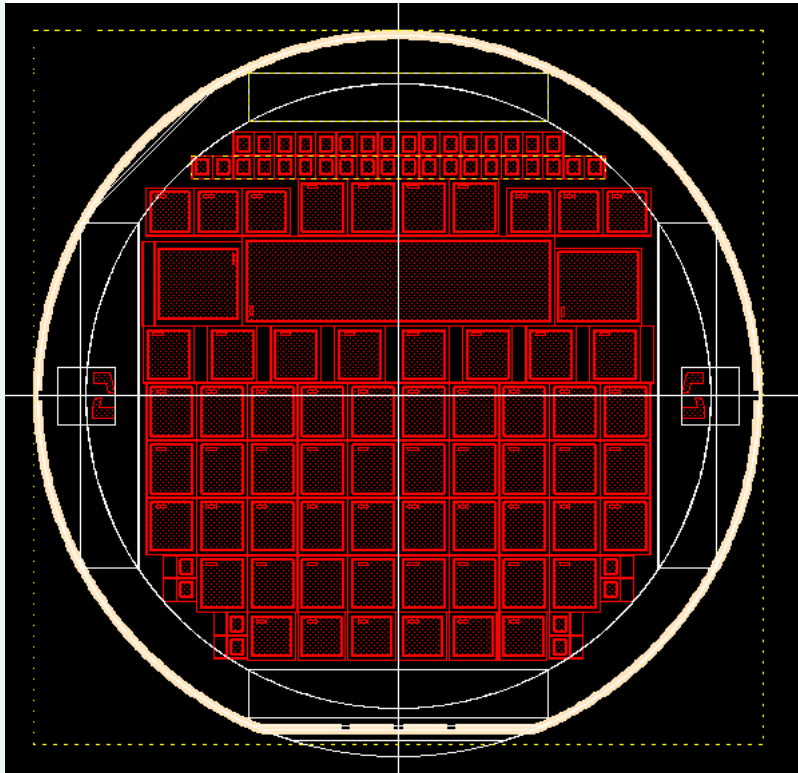
*Similar to results from n-type epi-material
with the same thickness (G.Kramberger):
3200e (62% average),
2400e (60% most probable).*

*N.B. At fluences around 10^{16} p/cm 2 the
signal collection is anyhow limited by
charge trapping to a few tens of μ m also
in thicker devices!*



Layout of the new production

Wafer layout – back side view



Back side oxidation and lithography under way at the moment at HLL!

Top Wafer Materials:

- ✓ Fz n-type, $\langle 100 \rangle$, $360 \Omega \cdot \text{cm}$, to be thinned down to $75 \mu\text{m}$
- ✓ Fz p-type, $\langle 100 \rangle$, $5 \text{K}\Omega \cdot \text{cm}$ to be thinned down to 75 and $150 \mu\text{m}$.
→ compare to epitaxial material within the RD50 Collaboration

Process:

- ✓ Use the same front side mask both for n- and p-type material
- ✓ Patterned p+ implantation on the back side only needed for n-on-n detectors → simplified process for p-type material!

Devices :

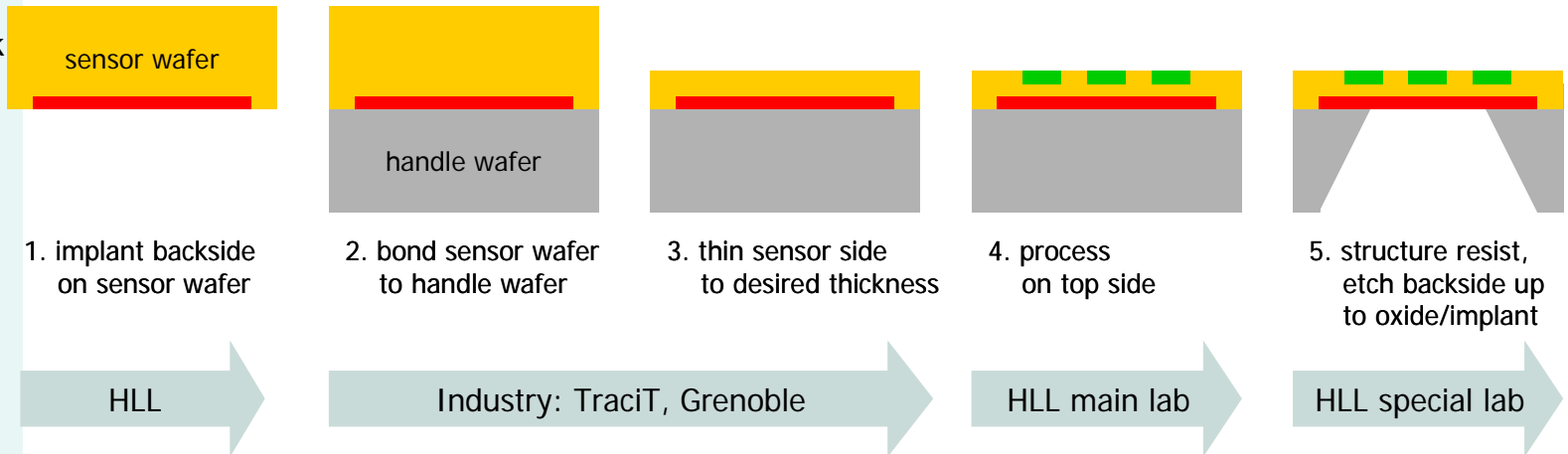
- ✓ Pixels with the same layout as the present Atlas pixel detector or reduced pitches (from $50 \times 400 \mu\text{m}^2$ to $50 \times 50 \mu\text{m}^2$) → Plan to read out pixels with reduced pitches by a customized ASIC from Interon AS, Norway
- ✓ Test-structures to optimize the pixel isolation technique (p-spray, moderated p-spray)



Thinning Technology

✓ Handle wafer of the same material as the top wafer, n- or p-type Fz

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✓ Deep anisotropic wet etching leaves rough surfaces → the process has been optimized to open the contacts and apply the metallization after etching of the handle wafer.

✓ Thin (50 μm) silicon already successfully produced at MPI.:

- MOS diodes.
- Small strip detectors.
- Mechanical dummies.

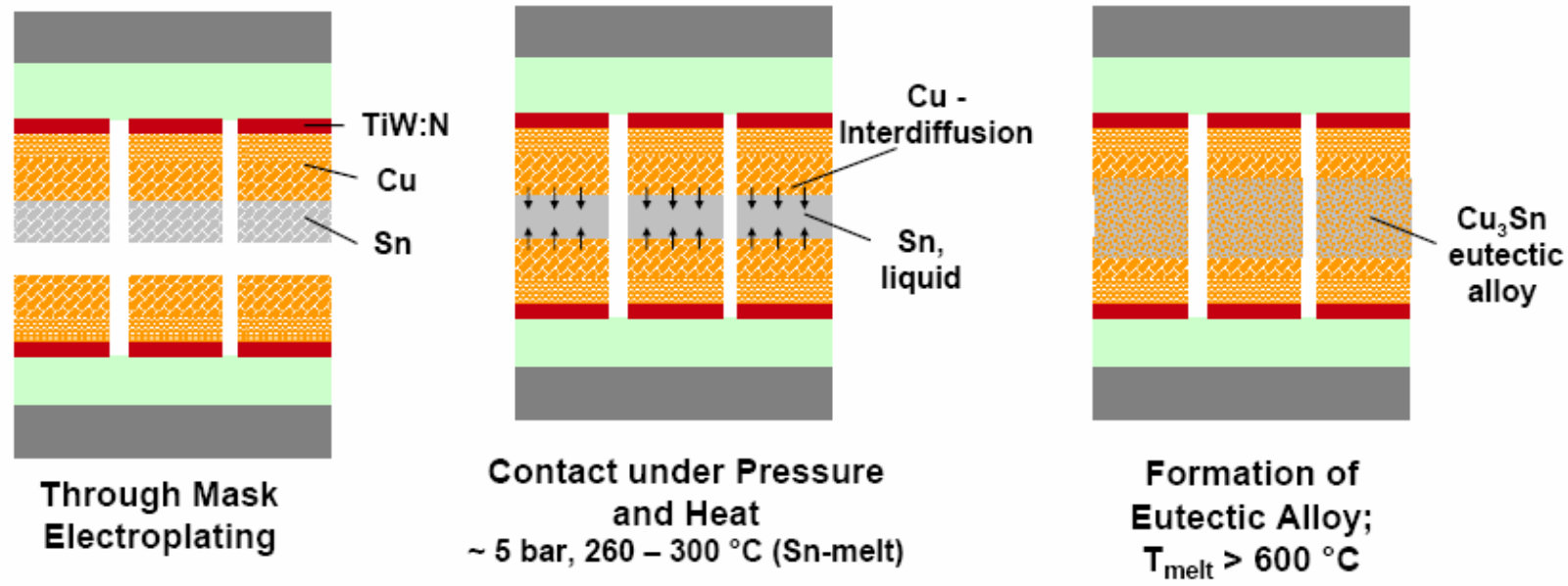
-No deterioration of detector properties, keep $I_{\text{leak}} < 100\text{pA/cm}^2$



IZM SLID Process

Metallization SLID (Solid Liquid Interdiffusion)

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- *Alternative to bump bonding (less process steps “potentially lower cost” (IZM)).*
- *Small pitch possible ($< 20 \mu\text{m}$, depending on pick & place precision).*
- *Stacking possible (next bonding process does not affect previous bond).*
- *Wafer to wafer and chip to wafer possible.*



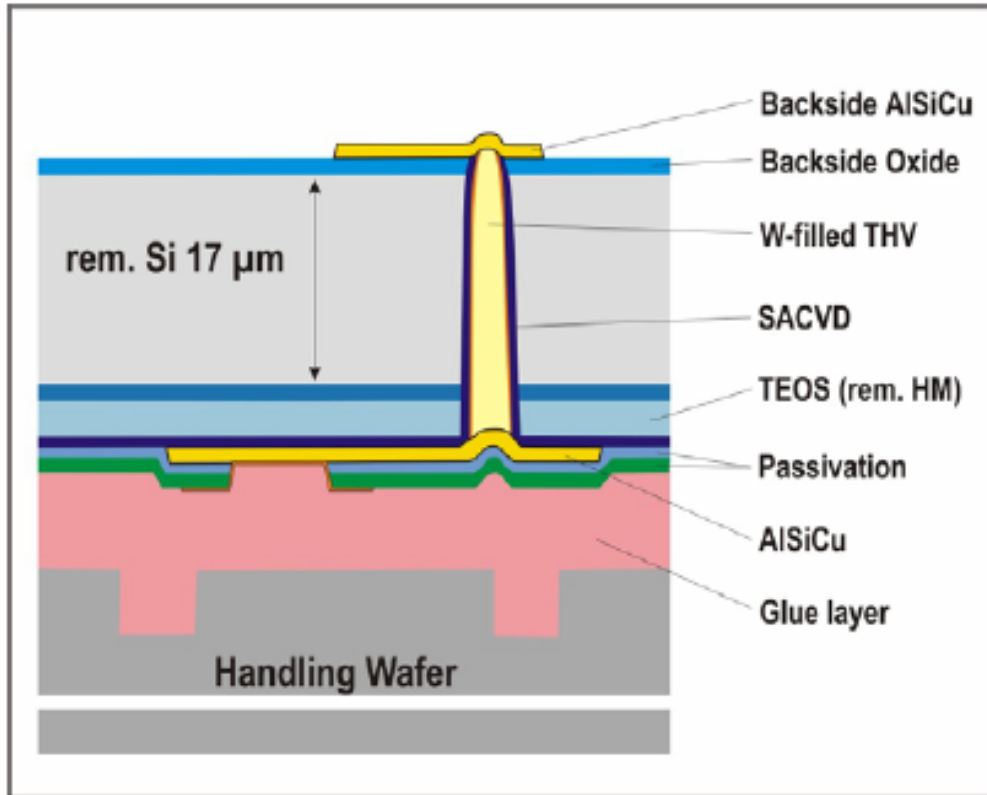
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Inter Chip Vias

IZM

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If you want to add a third layer or access the chip from the opposite side of the wafer ...



✓ Fabrication of Tungsten-filled InterChip Vias on top substrate:

- $2 \times 2 \mu\text{m}^2$

- aspect ratio 8:1, aim to reach 16:1

- 2.5 Ohm / per via

✓ Bonding to handling substrate and thinning

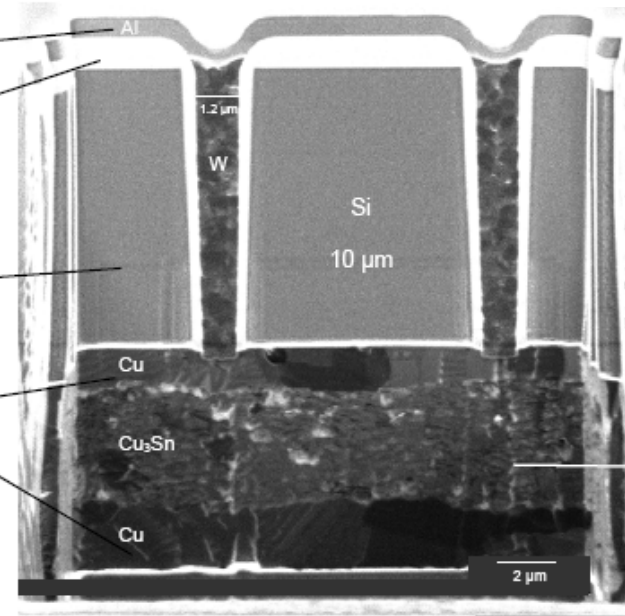
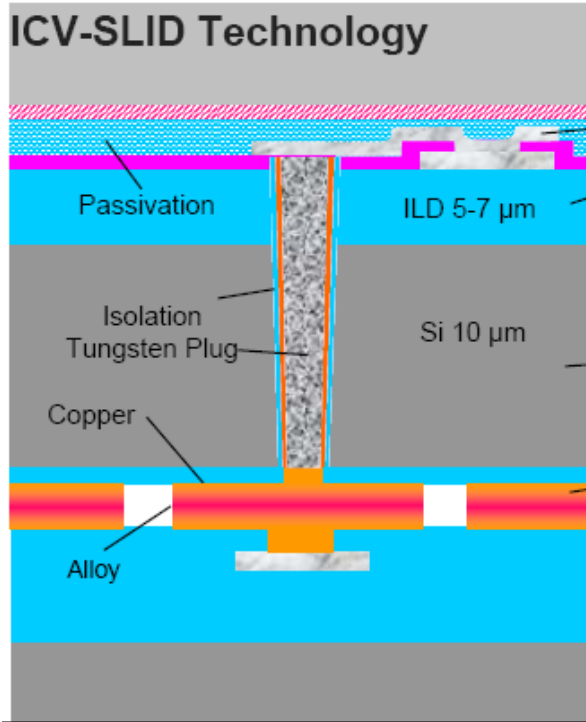
✓ Opening of plugs

✓ Through Mask Electroplating



Inter Chip Vias + Slid

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IZM

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- ✓ Alignment and soldering to the bottom wafer through SLID
- ✓ No significant impact on chip performance (tested at IZM on MOS transistors).

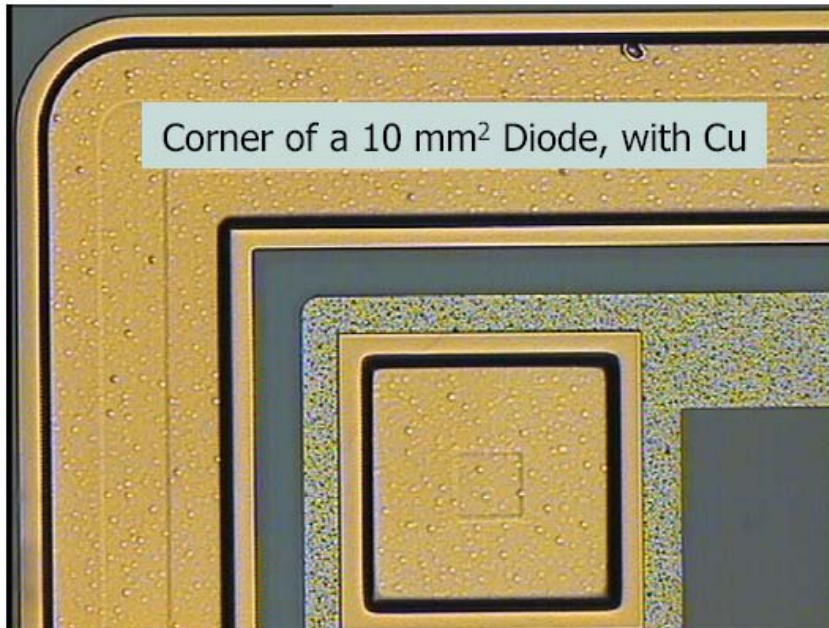


Results on the first test diodes (I)

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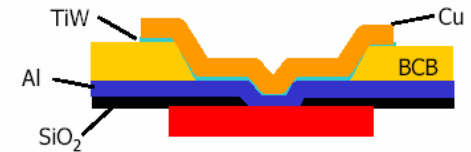


✓ BCB layer with openings to define
TiW/Cu/Sn systems



To be sure that the preparation of the sensor wafers for SLID does not degrade the sensors:

- simple diodes produced on SOI wafers:
- top layers 50 μm thick, $\rho=150 \Omega\cdot\text{cm}$



Metal system added at IZM \rightarrow simulation of SLID process without a real soldering of the two wafers :

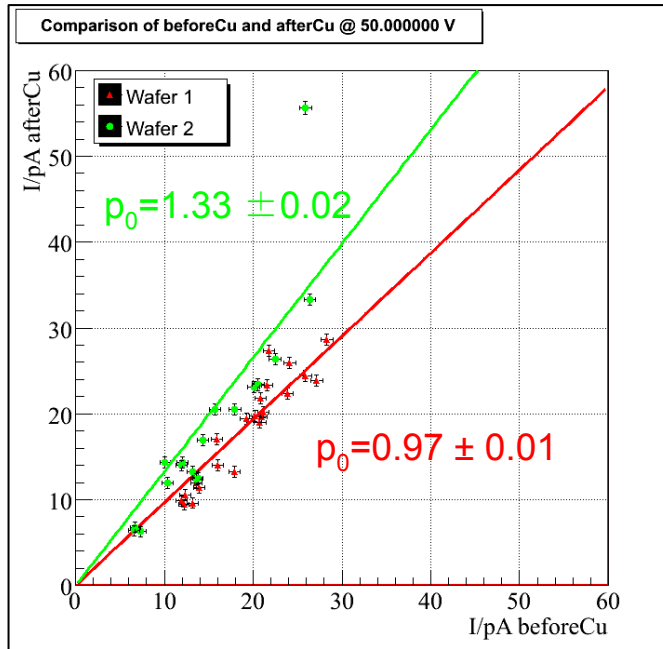
Wafer 1: TiW sputtering + Cu through mask electroplated + SLID temperature treatment

Wafer 2: TiW sputtering + Cu and Sn through mask electroplated + SLID temperature treatment



Results on the first test diodes (II)

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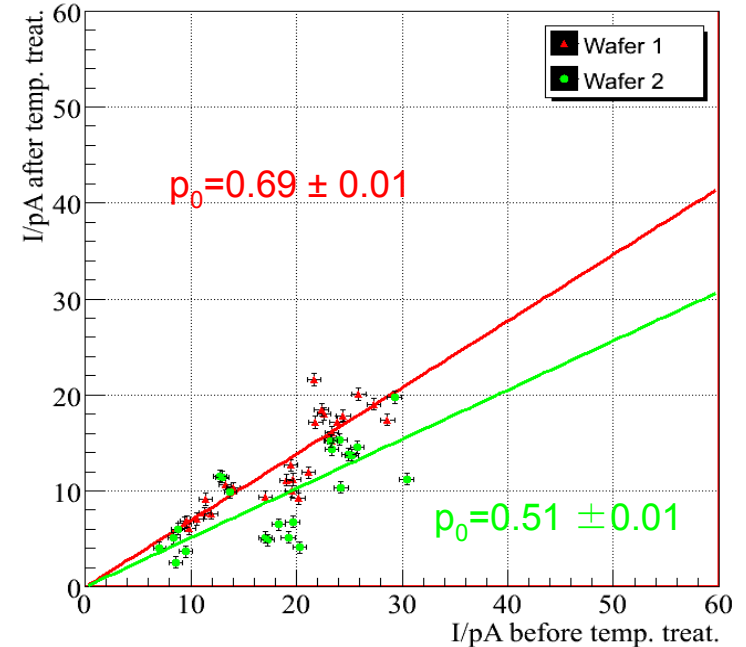
Correlation of the reverse current at full depletion (50 V) before and after Cu metallization

→ No significant effect noticeable

Correlation of the reverse current before and after SLID temperature treatment (around 300 °C) → slight decrease of the reverse current after the temperature treatment

Possible explanation: annealing by temperature treatment.

Dark currents before and after temp. treat.





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Conclusions

A new ATLAS R&D program has started on:

- ✓ *Thin FZ sensors (“standard” pixel sensors optimized for SLHC).*
- ✓ *3D interconnections:*
 - *Alternative to bump bonding.*
 - *Opening new possibilities for ASIC and module design.*

Modular R&D:

- ✓ *Thin sensors can be used with standard hybrid pixel ASICs (bump bonded).*
- ✓ *3D Interconnection is an option for other sensor types (e.g. 3D detectors).*

Status and perspectives:

- ✓ *The production of thin pixels on Fz material has started at HLL*
- ✓ *First tests of the SLID process on diodes*
- ✓ *Module demonstrator expected in 2008-2009*

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